

October 1987 Revised January 2004

MM74C906 Hex Open Drain N-Channel Buffers

General Description

The MM74C906 buffer employs monolithic CMOS technology in achieving open drain outputs. The MM74C906 consists of six inverters driving six N-channel devices. The open drain feature of these buffers makes level shifting or wire AND and wire OR functions by just the addition of pullup or pull-down resistors. All inputs are protected from static discharge by diode clamps to $\rm V_{CC}$ and to ground.

Features

■ Wide supply voltage range: 3V to 15V

■ Guaranteed noise margin: 1V

■ High noise immunity: 0.45 V_{CC} (typ.)

■ High current sourcing and sinking open drain outputs

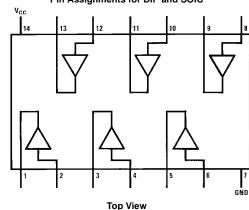
Ordering Code:

Order Number	Package Number	Package Description				
MM74C906M (Note 1)	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow				
MM74C906N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide				

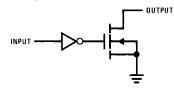
Note 1: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP and SOIC



Logic Diagram



Absolute Maximum Ratings(Note 2)

Voltage at Any Input Pin $-0.3 \mbox{V to V}_{\mbox{CC}} + 0.3 \mbox{V}$

Voltage at Any Output Pin

Operating Temperature Range -40°C to $+85^{\circ}\text{C}$ Storage Temperature Range -65°C to $+150^{\circ}\text{C}$

Power Dissipation

Dual-In-Line 700 mW Small Outline 500 mW

Operating V_{CC} Range 3V to 15V

Absolute Maximum V_{CC} 18V

Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units
CMOS TO	CMOS		.		I	
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 5V	3.5			V
		V _{CC} = 10V	8.0			V
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 5V			1.5	V
		$V_{CC} = 10V$			2	V
I _{IN(1)}	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1	μΑ
I _{IN(0)}	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μΑ
I _{CC}	Supply Current	V _{CC} = 15V, Output Open		0.05	15	μΑ
	Output Leakage					
		$V_{CC} = 4.75V, V_{IN} = V_{CC} - 1.5V$		0.005	5	μΑ
		$V_{CC} = 4.75V, V_{OUT} = 18V$				
CMOS/LP	ITL INTERFACE	•				
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 4.75V	V _{CC} – 1.5V			V
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 4.75V			0.8	V
OUTPUT D	DRIVE CURRENT	·				•
		$V_{CC} = 4.75V, V_{IN} = 1V + 0.1 V_{CC}$				
		$V_{CC} = 4.75V, V_{OUT} = 0.5V$	2.1	8.0		mA
		$V_{CC} = 4.75V, V_{OUT} = 1.0V$	4.2	12.0		mA
		$V_{CC} = 10V, V_{IN} = 2V$				
		$V_{CC} = 10V$, $V_{OUT} = 0.5V$	4.2	20		mA
		$V_{CC} = 10V$, $V_{OUT} = 1V$	8.4	30		mA

AC Electrical Characteristics (Note 3)

 $T_A = 25^{\circ}C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{pd}	Propagation Delay Time					
	to a Logical "0"					
		$V_{CC} = 5.0V, R = 10k$			150	ns
		V _{CC} =10V, R = 10k			75	ns
t _{pd}	Propagation Delay Time					
	to a Logical "1"					
		V _{CC} = 5.0V (Note 4)			150 + 0.7 RC	ns
		V _{CC} = 10V (Note 4)			75 + 0.7 RC	ns
C _{IN}	Input Capacitance	(Note 5)		5.0		pF
C _{OUT}	Output Capacity	(Note 5)		20		pF
C _{PD}	Power Dissipation Capacity	(Note 6) Per Buffer		30		pF

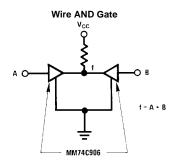
Note 3: AC Parameters are guaranteed by DC correlated testing.

Note 4: "C" used in calculating propagation includes output load capacity (C_L) plus device output capacity (C_{OUT}).

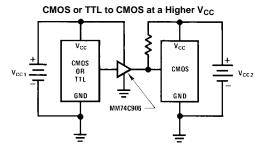
Note 5: Capacitance is guaranteed by periodic testing.

Note 6: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note, AN-90. (Assumes outputs are open).

Typical Applications



Note: Can be extended to more than 2 inputs.



Physical Dimensions inches (millimeters) unless otherwise noted $\frac{0.335 - 0.344}{(8.509 - 8.738)}$ LEAD NO. 1 IDENT $\frac{0.150 - 0.157}{(3.810 - 3.988)}$ $\frac{0.010-0.020}{(0.254-0.508)}$ $\frac{0.053 - 0.069}{(1.346 - 1.753)}$ 8° MAX TYP ALL LEADS $\frac{0.004 - 0.010}{(0.102 - 0.254)}$ SEATING PLANE 0.014 (0.356) 0.008 - 0.010 (0.203 - 0.254) TYP ALL LEADS $\frac{0.014 - 0.020}{(0.356 - 0.508)} \text{ TYP}$ 0.050 (1.270) TYP 0.016 - 0.050 (0.406 - 1.270) TYP ALL LEADS 0.004 (0.102) ALL LEAD TIPS $\frac{0.008}{(0.203)}$ TYP

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770(18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 0.250 ± 0.010 PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\overline{(7.620 - 8.128)}$ 0.065 $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 0.060 4° TYP Optional (1.524) (1.651) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ 0.280 (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) TYP (0.356 - 0.584)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

 $\frac{0.050\pm0.010}{(1.270-0.254)}$ TYP

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 $0.325 + 0.040 \\ -0.015 \\ \hline (8.255 + 1.016) \\ -0.381)$

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N144 (REV.E)